



DVCS Calorimeter Trigger

Version 2014

Laboratoire de Physique Corpusculaire
de Clermont-Ferrand
CNRS - IN2P3 / Université Blaise Pascal

Auteur

Magne Magali

Réf.

AAAAA

Date

09/05/2014

DVCS Calorimeter Trigger Version 2014

Electronic

DRAFT

Version: May 2014

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1. The Calorimeter trigger system

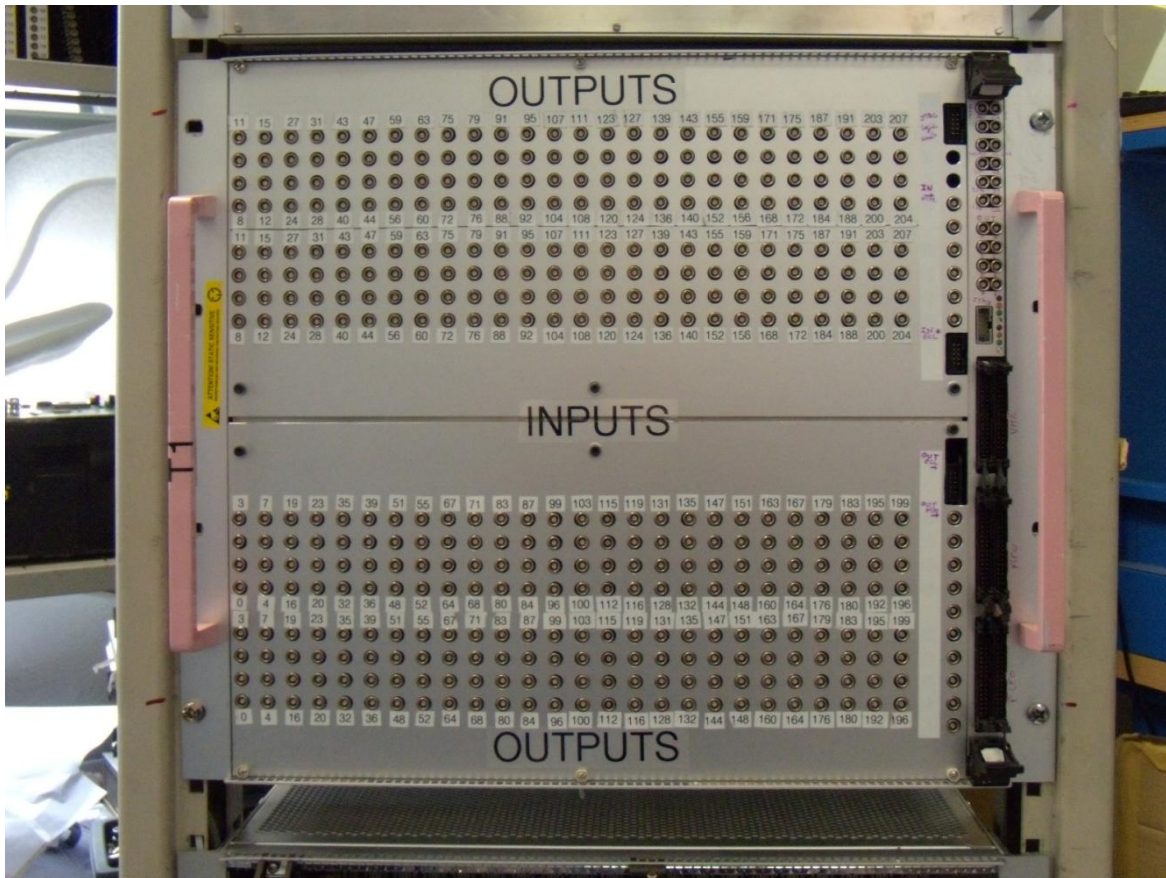


Figure 1 trigger box 2014

The hardware design begins in 2007 for the DVCS experiment in 2010 at JLAB.

The first version is composing by:

- the Vme_control boards which permit to interface the trigger box to the VME crate CPU.
- The daughter boards, which integrate 4 signals during a door and convert it in numeric data, to the mother boards. 52 boards are needed to cover the 208 channel of the calorimeter.
- The Trigger_mother board in version 2010 which make the data processing of the data come from the daughter boards.



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- The trigger_IO board which permit to have in front panel of the box input and output for the trigger logic, Jtag chain, and interface the mother board to the Vme_CTRL Board.

For the DVCS 2014 experiment:

Something have been increased.

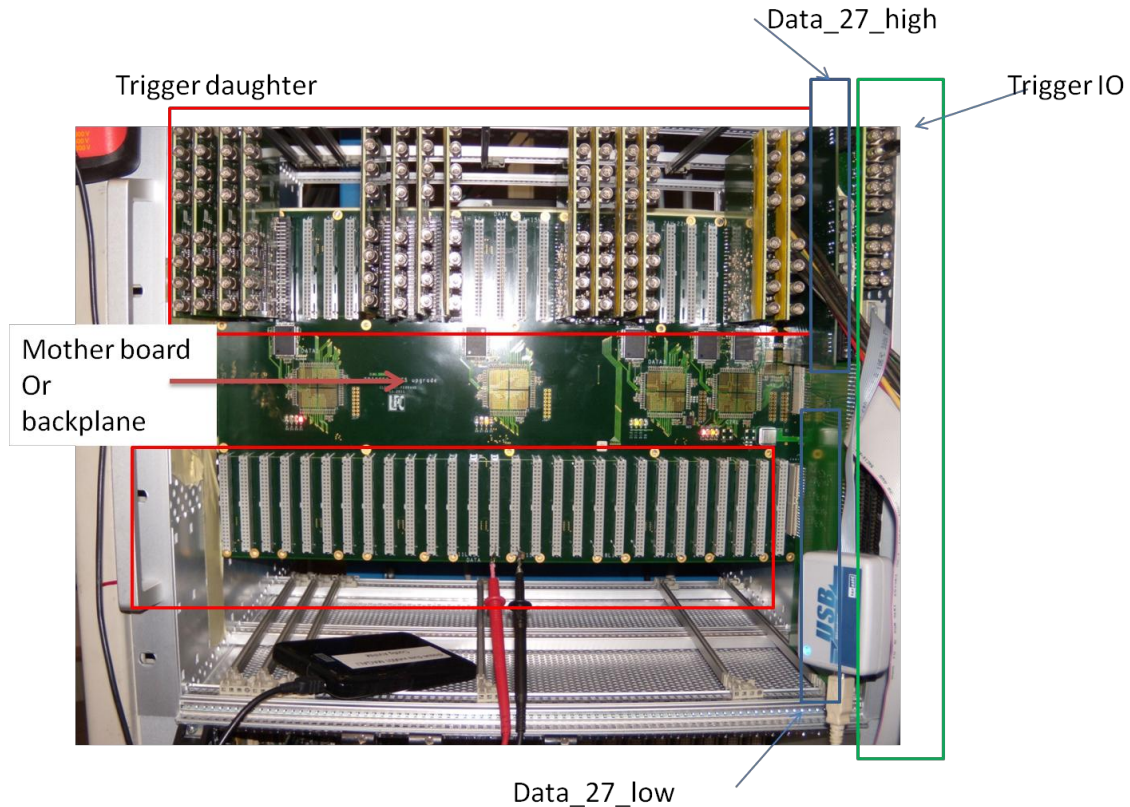


Figure 2 Trigger box 2014 boards names

- the Vme_control boards stay the same : only firmware upgrade to permit to replace VME standard protocol to BLT Protocol to increase the data rate acquisition.
- The daughter boards: only 2 resistors values by channel have been change to permit to have the well windows capture and permit to increase the resolution. (Before the windows is too bigger).
- The Trigger_mother board has been re-design to permit to solve something view during the experiment 2010.
- The trigger_IO: same board.



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- Adding board: The Data27H board and The Data27L board: this boards used daughter boards slot, this boards permit to have more Inputs and outputs NIM and ECL format.

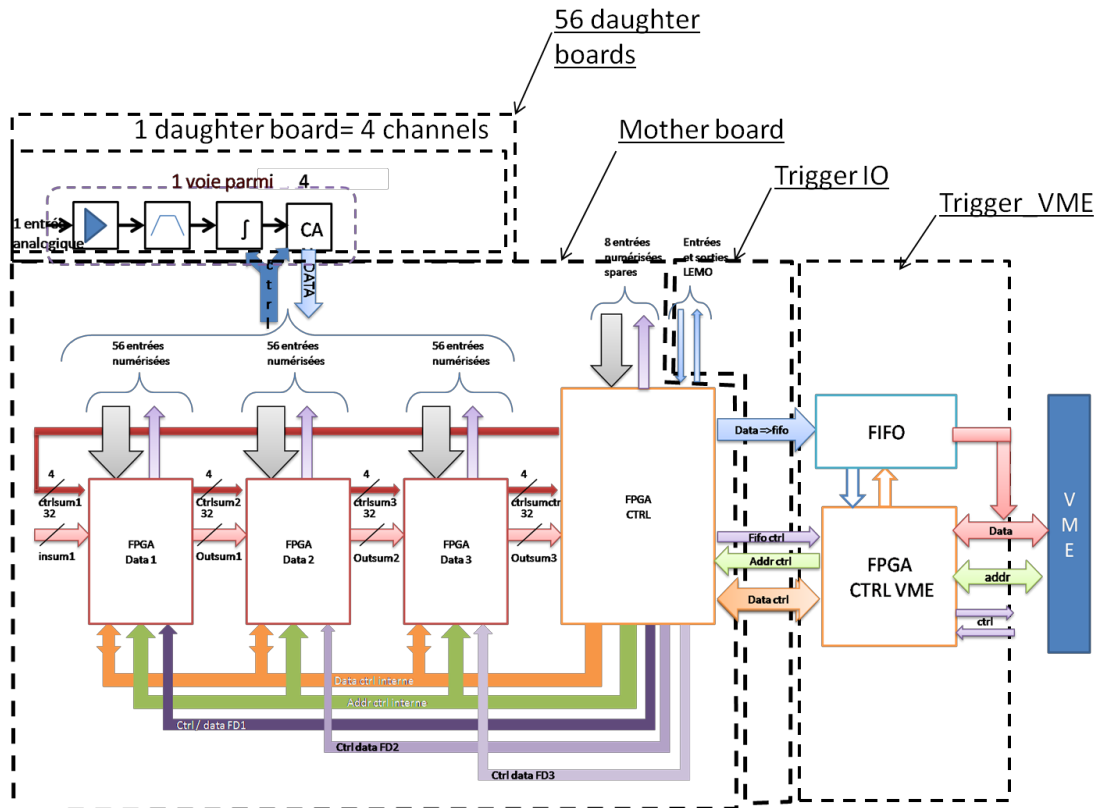


Figure 3 Trigger diagram



2. The VME_control Board

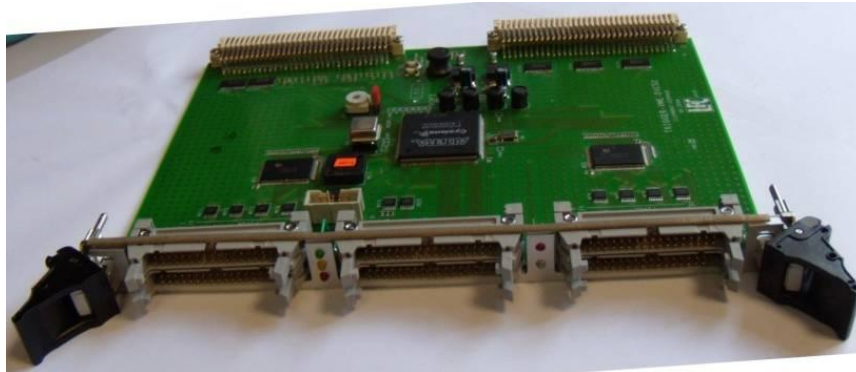


Figure 4 VME_ctrl board picture

a. The electronic board:

It's a VME 6U board based on a FPGA (Cyclone 1 ALTERA)
The goal of this board is to send data come from the trigger box to the VME CPU.

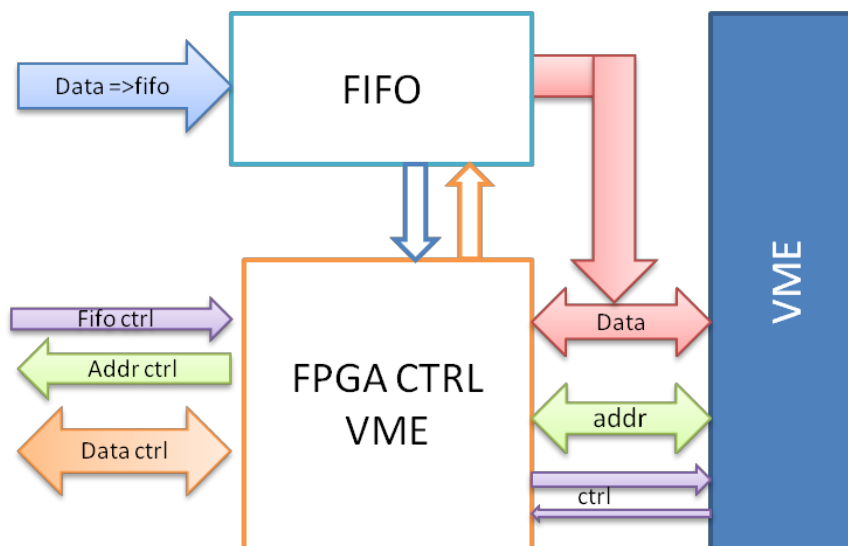


Figure 5 Vme_ctrl diagram

The data can go to the the VME CPU by two way :

- one by the fifo (2 bus of 32 bits double connector high and low of the board) but not used.
- The second way is by the VME Bus motnitored by the FPGA .



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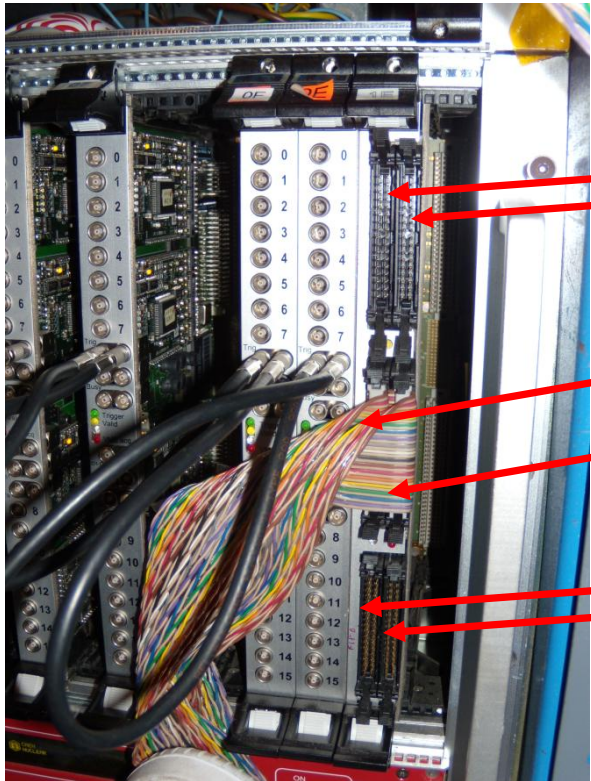
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b. Front panel:



Not used

To Trigger BOX

Connector VME RIGH
and Left
Cable 34 contacts

Not used

This board is address in VME A24 D32 protocol and A24 BLT protocol to the data acquisiti



3. Daughter boards

The daughter board has two functionalities.

The first is to receive 4 signals come from the calorimeter and duplicate it to send the analog to the sampling board(ARS16VME64 boards)

The second is to detect at each first level trigger if something occurs in each channel. To do that each channel are integrated and the result is digitized to be processing by the mothe board.



Figure 6 daughter electronic board

These boards permit to integrate positive and negative signal. The configuration signals are generated by the mother board (ctrl_FPGA).

2 type of signal are needed:

The gate for the integrator: this signal can have a parametric width and delay between the level 1 trigger. It's permit to adapt in time of the input signal arrival.

The multiplexing ADC output data are needed, because in goal to reduce the numbers of wire transit between the daughter board and the mother board, I have multiplexing the data (signal OE1/OE2/OE3/OE4/CLK).



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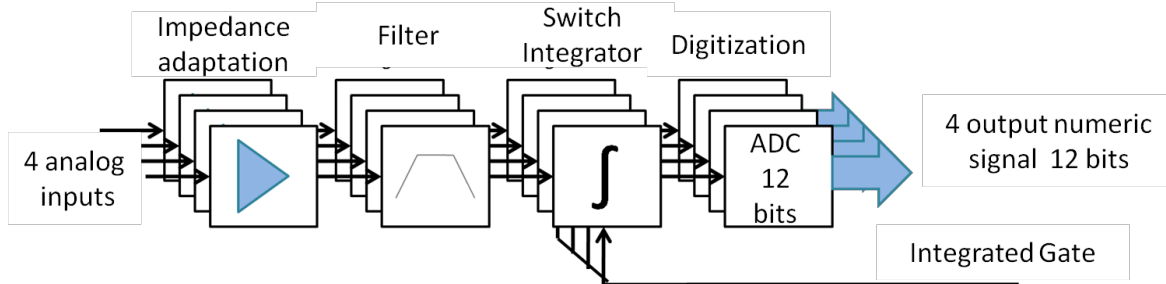


Figure 7 Daughter board diagram

The figure bellows shows in the result of integrated signal during a gate for a positive and a negative signal.

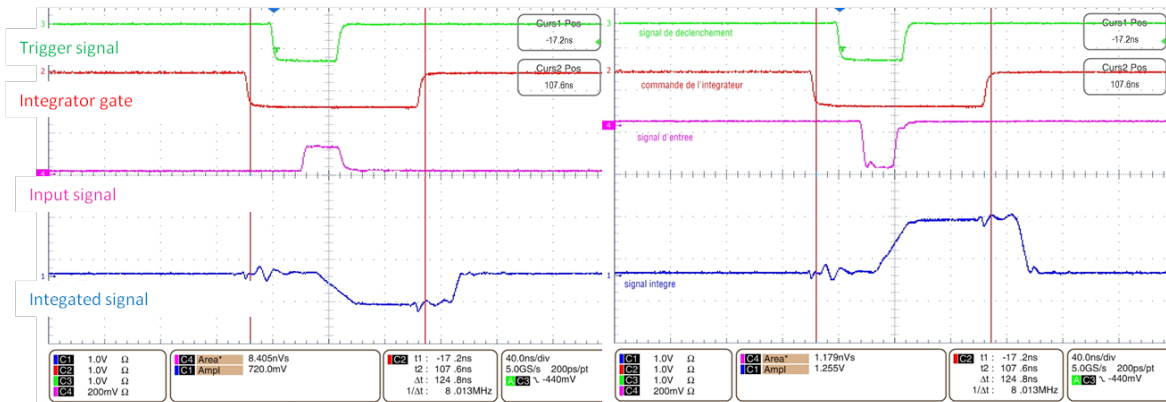


Figure 8 daughter board signal capture

The sampling is done all the time at each rising clock but the mother board acquires only the value at the end of the integrated gate.

The resolution of ADC versus integrator is around 12 pVs.

$$12\text{pVs} * 2048(\text{positive part} = \text{half ADC}) = 24 \text{ nVs}$$

To have an idea :

$$1 \text{ ARS ADC step is } 1\text{ns} * 0.6 \text{ mV} \rightarrow 0.6 \text{ pVs}$$

Amplitude max of a signal view by an ARS board is 600mV.

If the gate is 60 ns (width previously used for the 2010 experiment).

$$\rightarrow \text{max you have } 60 \text{ ns} * 600\text{mV} = 36 \text{ nVs,}$$

But the gate never be full except when you a very high signal.



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A typical signal is around an integral 21000 ARS LSB

Equal to 12, 6nVS < 24 nVs offer by the trigger integration windows.



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4. The mother boards (backplane)



5. The Trigger_Io_board

This board has for functionality to add more Numeric Inputs/outputs connectors on the front panel of the trigger box.

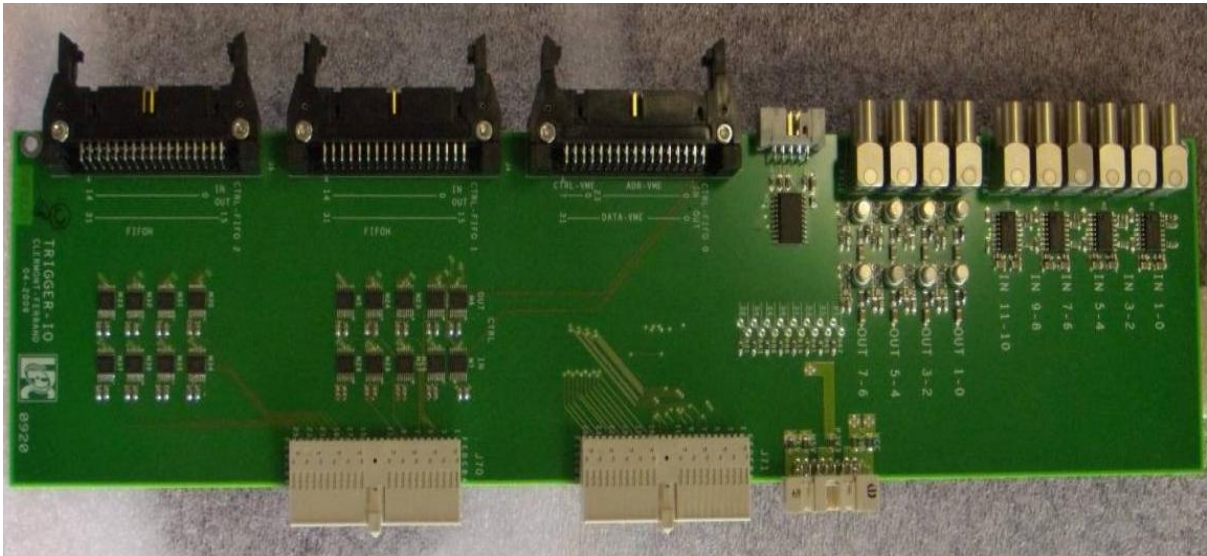


Figure 9 Tigger_IO Board

This board includes:

- 12 NIM to TTL converter

- 8 TTL to NIM converters

The Jtag input connector for the main jtag chain of the mother board.

The interface for the DATA signal between the mother board to the ribbon cable to the VME CTRL board.

And also the added JTAG chain connector for the logic unit FPGA of the mother board.



6. The Data27H board

This board has for functionality to add more Numeric Inputs on the front panel of the trigger box.

This added board is pug on the slot 27H of the mother board (previously used for daughter board spares)

Logic unit
Jtag chain
connector

6 NIM
INPUTS

4 ECL
INPUTS

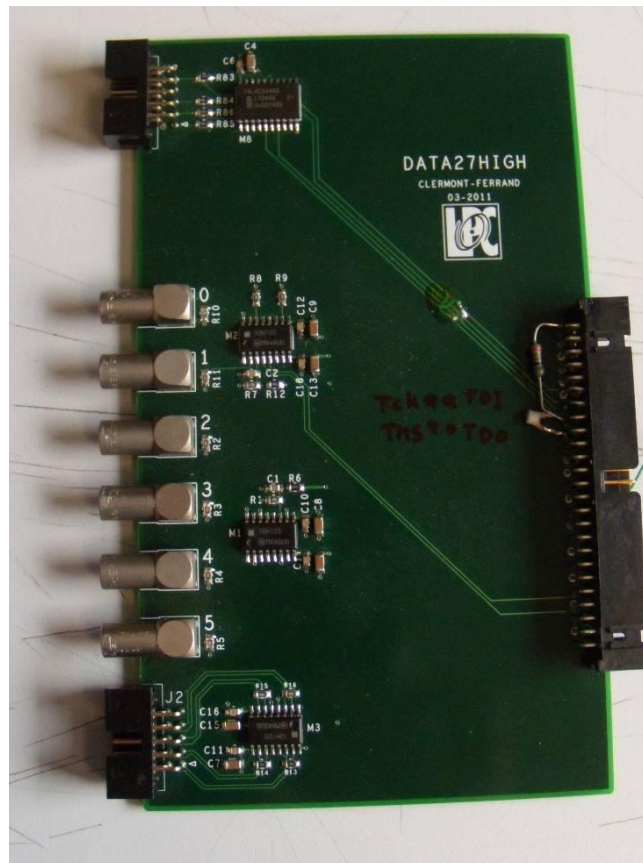


Figure 10 Data27H board

This board includes 6 NIM to TTL converter and 4 ECL to TTL converters. And also the added JTAG chain connector for the logic unit FPGA of the mother board.



7. The Data27L board

This board has for functionality to add more Numeric Outputs on the front panel of the trigger box.
This added board is pug on the slot 27L of the mother board
(previously used for daughter board spares)

10 NIM
outputs

4 ECL
outputs

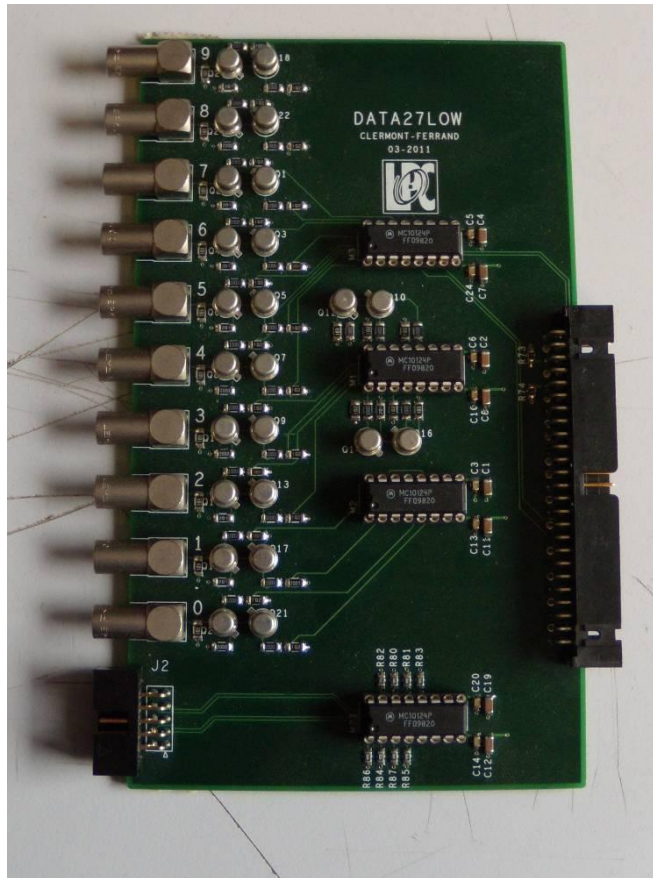


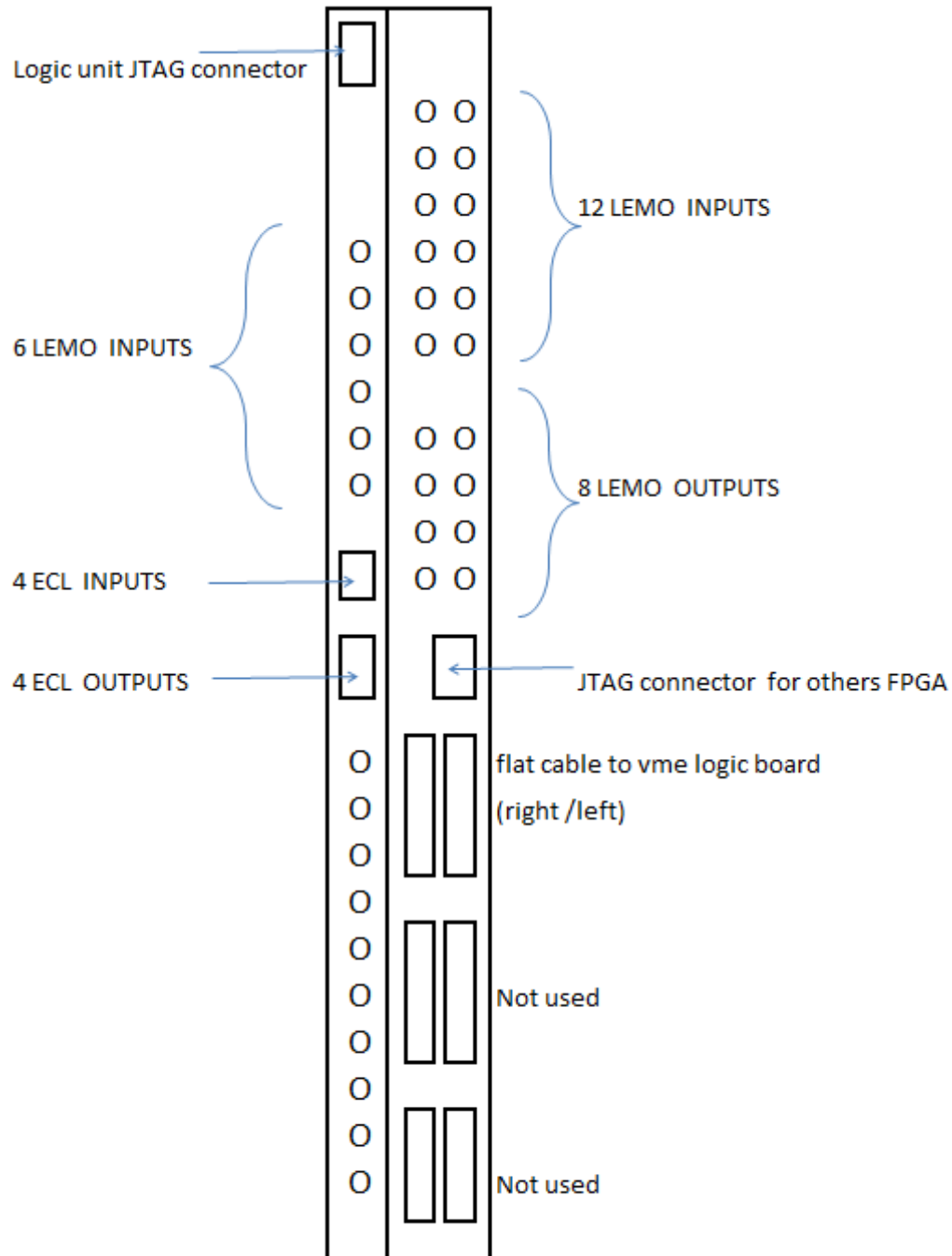
Figure 11 Data27L board

This board includes 10 TTL to NIM converter and 4 TTL to ECL converters.



8. Trigger Box connectors

Right part view include all the IO come from the boards:
trigger_IO / Data27H and Data27L





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The IO come from the Trigger_IO board are already defined.

It's the same of the previous trigger version
Part right:

The adding input and outputs lemo and ecl are not defined at the



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Calorimeter versus trigger inputs

a. Calorimeter

15	31	47	63	79	95	111	127	143	159	175	191	207
14	30	46	62	78	94	110	126	142	158	174	190	206
13	29	45	61	77	93	109	125	141	157	173	189	205
12	28	44	60	76	92	108	124	140	156	172	188	204
11	27	43	59	75	91	107	123	139	155	171	187	203
10	26	42	58	74	90	106	122	138	154	170	186	202
9	25	41	57	73	89	105	121	137	153	169	185	201
8	24	40	56	72	88	104	120	136	152	168	184	200
7	23	39	55	71	87	103	119	135	151	167	183	199
6	22	38	54	70	86	102	118	134	150	166	182	198
5	21	37	53	69	85	101	117	133	149	165	181	197
4	20	36	52	68	84	100	116	132	148	164	180	196
3	19	35	51	67	83	99	115	131	147	163	179	195
2	18	34	50	66	82	98	114	130	146	162	178	194
1	17	33	49	65	81	97	113	129	145	161	177	193
0	16	32	48	64	80	96	112	128	144	160	176	192



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b. Trigger inputs and board mezzanine reference

input

11	15	27	31	43	47	59	63	75	79	91	95	107	111	123	127	139	143	155	159	171	175	187	191	203	207
10	14	26	30	42	46	58	62	74	78	90	94	106	110	122	126	138	142	154	158	170	174	186	190	202	206
9	13	25	29	41	45	57	61	73	77	89	93	105	109	121	125	137	141	153	157	169	173	185	189	201	205
8	12	24	28	40	44	56	60	72	76	88	92	104	108	120	124	136	140	152	156	168	172	184	188	200	204

3	7	19	23	35	39	51	55	67	71	83	87	99	103	115	119	131	135	147	151	163	167	179	183	195	199
2	6	18	22	34	38	50	54	66	70	82	86	98	102	114	118	130	134	146	150	162	166	178	182	194	198
1	5	17	21	33	37	49	53	65	69	81	85	97	101	113	117	129	133	145	149	161	165	177	181	193	197
0	4	16	20	32	36	48	52	64	68	80	84	96	100	112	116	128	132	144	148	160	164	176	180	192	196

nom des mezzanines

0H	1H	2H	3H	4H	5H	6H	7H	8H	9H	10H	11H	12H	13H	14H	15H	16H	17H	18H	19H	20H	21H	22H	23H	24H	25H
0L	1L	2L	3L	4L	5L	6L	7L	8L	9L	10L	11L	12L	13L	14L	15L	16L	17L	18L	19L	20L	21L	22L	23L	24L	25L



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c. Trigger inputs and board mezzanine reference versus FPGA and VHDL assignments

version fpga

11	15	27	31	43	47	59	63	75	79	11	15	27	31	43	47	59	63	11	15	27	31	43	47	59	63		
10	14	26	30	42	46	58	62	74	78	10	14	26	30	42	46	58	62	10	14	26	30	42	46	58	62		
9	13	25	29	41	45	57	61	73	77	9	13	25	29	41	45	57	61	9	13	25	29	41	45	57	61		
8	12	24	28	40	44	56	60	72	76	8	12	24	28	40	44	56	60	8	12	24	28	40	44	56	60		
3	7	19	23	35	39	51	55	67	71	3	7	19	23	35	39	51	55	3	7	19	23	35	39	51	55		
2	6	18	22	34	38	50	54	66	70	2	6	18	22	34	38	50	54	2	6	18	22	34	38	50	54		
1	5	17	21	33	37	49	53	65	69	1	5	17	21	33	37	49	53	1	5	17	21	33	37	49	53		
0	4	16	20	32	36	48	52	64	68	0	4	16	20	32	36	48	52	0	4	16	20	32	36	48	52		

0H	1H	2H	3H	4H	5H	6H	7H	8H	9H	0H	1H	2H	3H	4H	5H	6H	7H	0H	1H	2H	3H	4H	5H	6H	7H
0L	1L	2L	3L	4L	5L	6L	7L	8L	9L	0L	1L	2L	3L	4L	5L	6L	7L	0L	1L	2L	3L	4L	5L	6L	7L



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d. Calorimeter versus FPGA

 FPGA1

 FPGA2

 FPGA3

15	31	47	63	79	95	111	127	143	159	175	191	207
14	30	46	62	78	94	110	126	142	158	174	190	206
13	29	45	61	77	93	109	125	141	157	173	189	205
12	28	44	60	76	92	108	124	140	156	172	188	204
11	27	43	59	75	91	107	123	139	155	171	187	203
10	26	42	58	74	90	106	122	138	154	170	186	202
9	25	41	57	73	89	105	121	137	153	169	185	201
8	24	40	56	72	88	104	120	136	152	168	184	200
7	23	39	55	71	87	103	119	135	151	167	183	199
6	22	38	54	70	86	102	118	134	150	166	182	198
5	21	37	53	69	85	101	117	133	149	165	181	197
4	20	36	52	68	84	100	116	132	148	164	180	196
3	19	35	51	67	83	99	115	131	147	163	179	195
2	18	34	50	66	82	98	114	130	146	162	178	194
1	17	33	49	65	81	97	113	129	145	161	177	193
0	16	32	48	64	80	96	112	128	144	160	176	192

e. Calorimeter versus FPGA and VHDL assignments

 FPGA1

 FPGA2

 FPGA3

15	31	47	63	79	15	31	47	63	15	31	47	63
14	30	46	62	78	14	30	46	62	14	30	46	62
13	29	45	61	77	13	29	45	61	13	29	45	61
12	28	44	60	76	12	28	44	60	12	28	44	60
11	27	43	59	75	11	27	43	59	11	27	43	59
10	26	42	58	74	10	26	42	58	10	26	42	58
9	25	41	57	73	9	25	41	57	9	25	41	57
8	24	40	56	72	8	24	40	56	8	24	40	56
7	23	39	55	71	7	23	39	55	7	23	39	55
6	22	38	54	70	6	22	38	54	6	22	38	54
5	21	37	53	69	5	21	37	53	5	21	37	53
4	20	36	52	68	4	20	36	52	4	20	36	52
3	19	35	51	67	3	19	35	51	3	19	35	51
2	18	34	50	66	2	18	34	50	2	18	34	50
1	17	33	49	65	1	17	33	49	1	17	33	49
0	16	32	48	64	0	16	32	48	0	16	32	48

moment.



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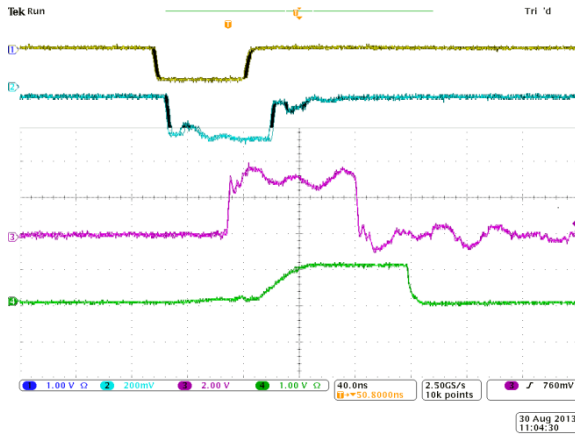
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9. ANNEXES

a. Typical trigger signals



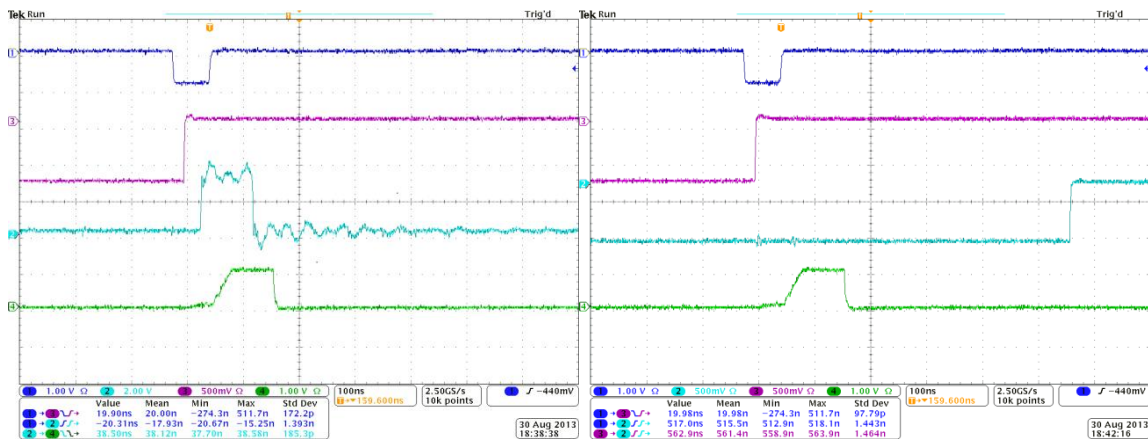
1 - trigger cosmic

2 - Analog input signal
(example channel 16)

3 - gate for integrated signal

4 - analog integrated signal

Timing ARS_stop/ ARS_start /Gate /signal integer



1 -cosmic trigger

2 - Ars_stop

3 - Gate (left plot) - ARS_start (right)

4 - analog integrated signal