DVCS Calorimeter Trigger
Version 2014

Electronic

DRAFT

Version: May 2014

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1. The Calorimeter trigger system

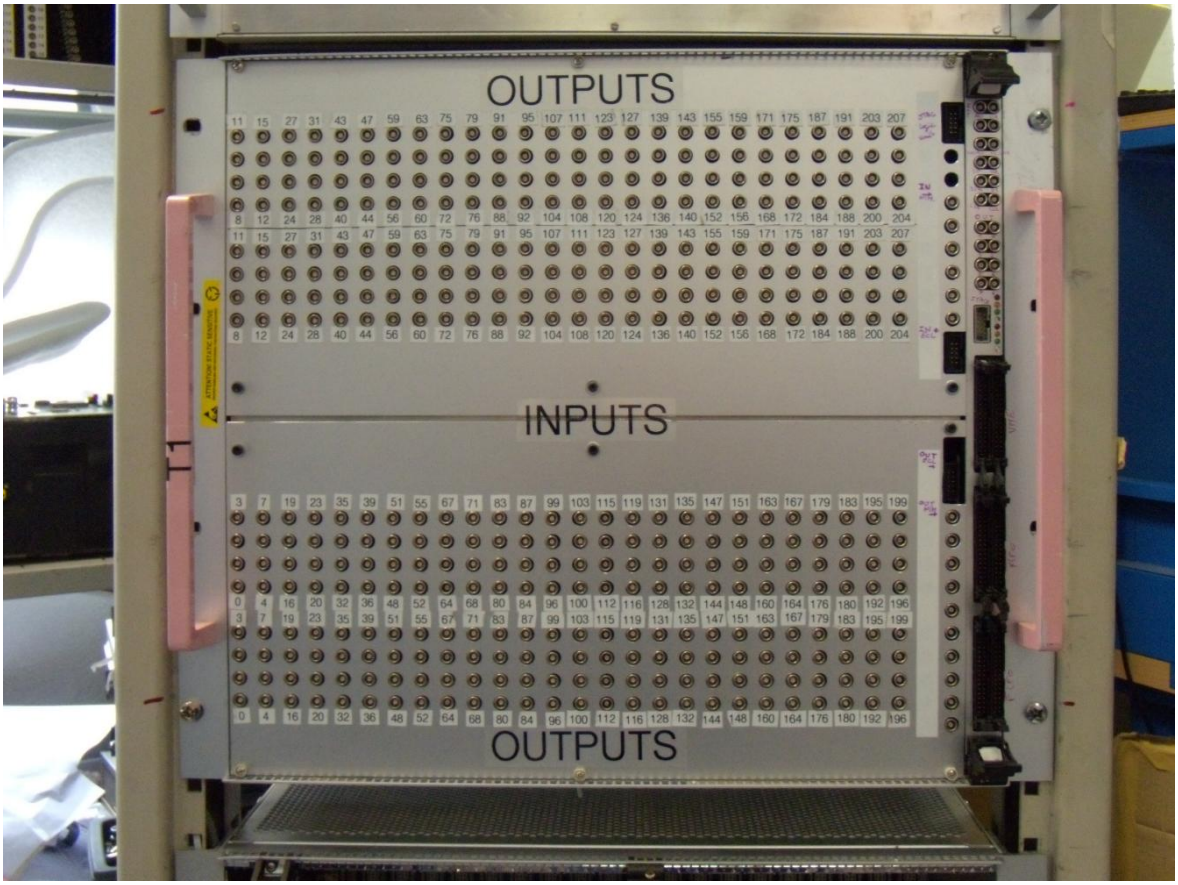

Figure 1 trigger box 2014

The hardware design begins in 2007 for the DVCS experiment in 2010 at JLAB.
The first version is composing by:

- the Vme_control boards which permit to interface the trigger box to the VME crate CPU.

- The daughter boards, which integrate 4 signals during a door and convert it in numeric data, to the mother boards.52 boards are needed to caver the 208 channel of the calorimeter.

- The Trigger_mother board in version 2010 which make the data processing of the data come from the daughter boards.

- The trigger_IO board which permit to have in front panel of the box input and output for the trigger logic, Jtag chain , and interface the mother board to the Vme_CTRL Board.

For the DVCS 2014 experiment:

Something have been increased.

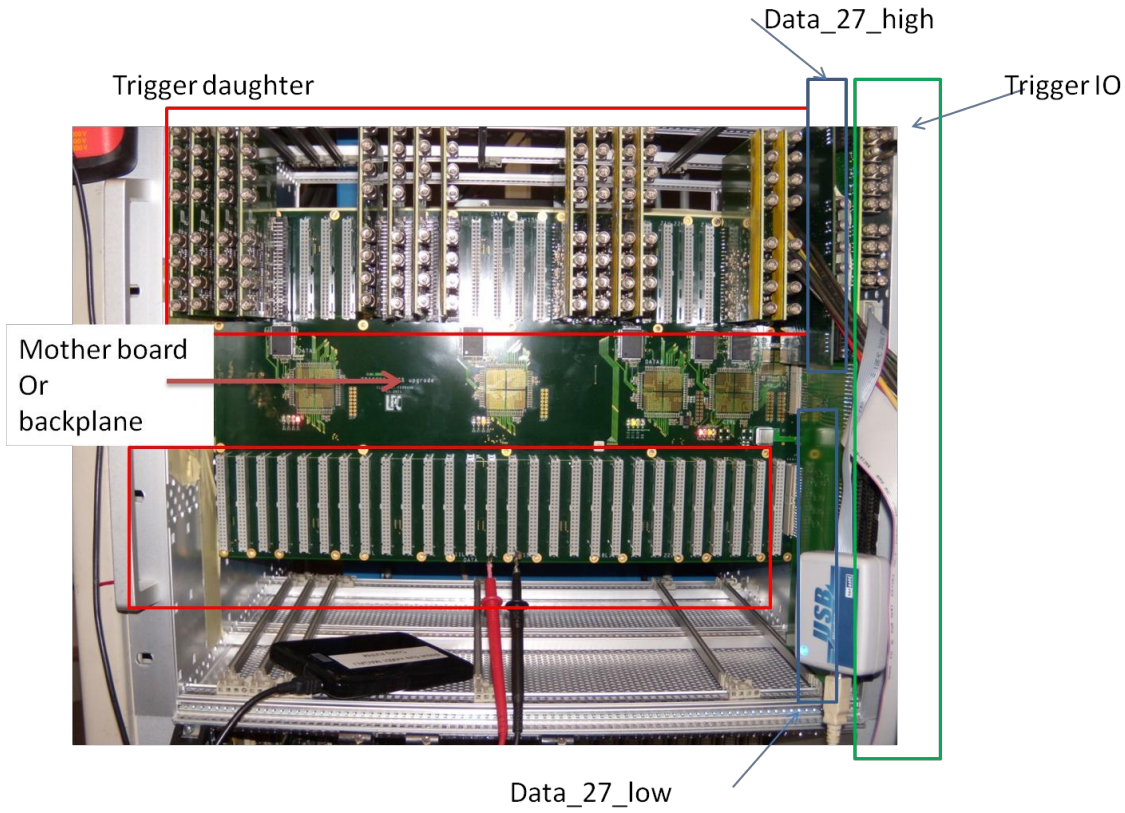

Figure 2 Trigger box 2014 boards names

- the Vme_control boards stay the same : only firmware upgrade to permit to replace VME standard protocol to BLT Protocol to increase the data rate acquisition.

- The daughter boards: only 2 resistors values by channel have been change to permit to have the well windows capture and permit to increase the resolution. (Before the windows is too bigger).

- The Trigger_mother board has been re-design to permit to solve something view during the experiment 2010.

- The trigger_IO: same board.

- Adding board: The Data27H board and The Data27L board: this boards used daughter boards slot, this boards permit to have more Inputs and outputs NIM and ECL format.

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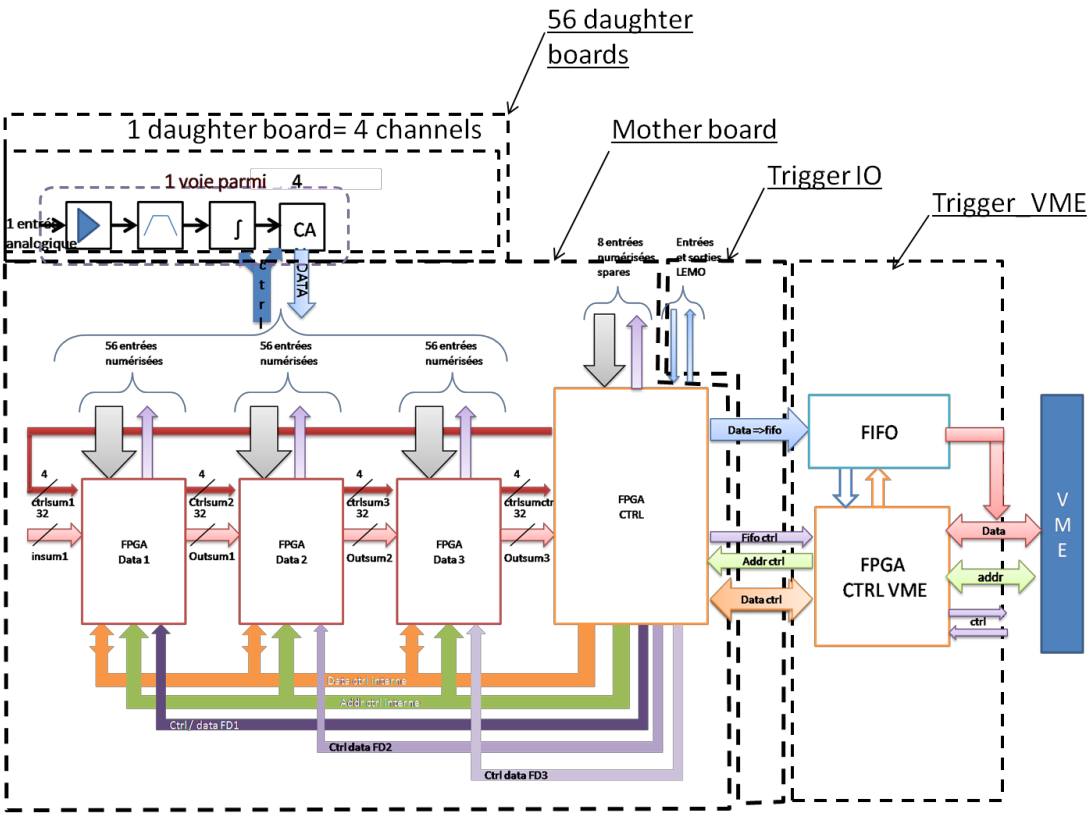


Figure 3 Trigger diagram

2. The VME_control Board

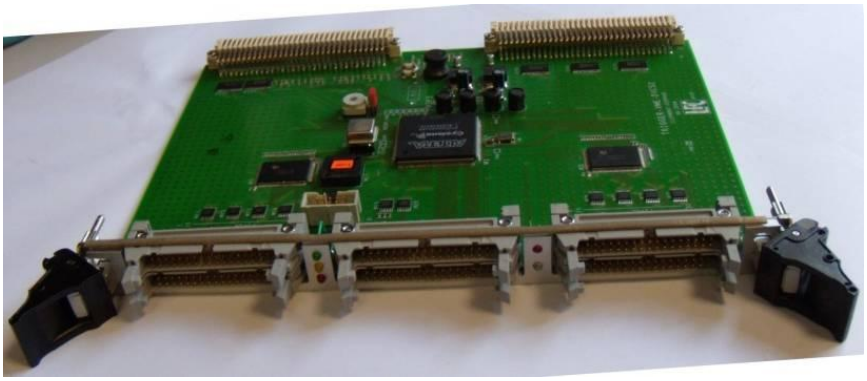


Figure 4 VME_ctrl board picture

a. *The electronic board:*

It's a VME 6U board based on a FPGA (Cyclone 1 ALTERA)
The goal of this board is to send send data come from the trigger box to the VME CPU.

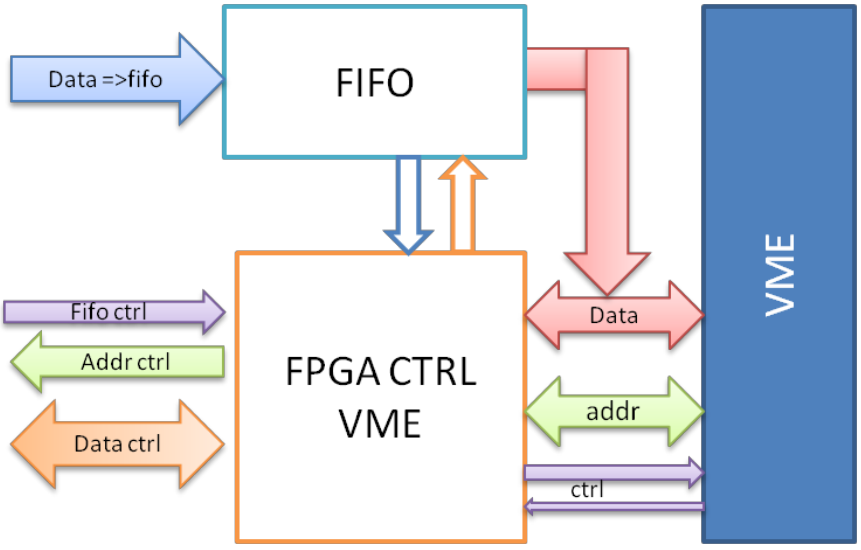
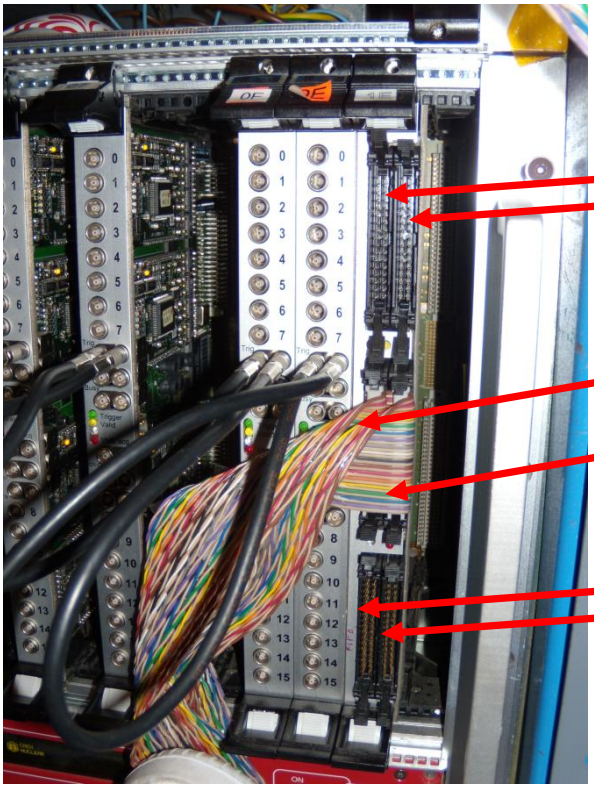


Figure 5 Vme_ctrl diagram

The data can go to the the VME CPU by two way :
- one by the fifo (2 bus of 32 bits double connector high and low of the board) but not used.
- The second way is by the VME Bus motnitored by the FPGA .

b. Front panel:



This board is address in VME A24 D32 protocol and A24 BLT protocol to the data acquisiti

3. Daughter boards

The daughter board has two functionalities.

The first is to receive 4 signals come from the calorimeter and duplicate it to send the analog to the sampling board(ARS16VME64 boards)

The second is to detect at each first level trigger if something occurs in each channel. To do that each channel are integrated and the result is digitized to be processing by the mothe board.

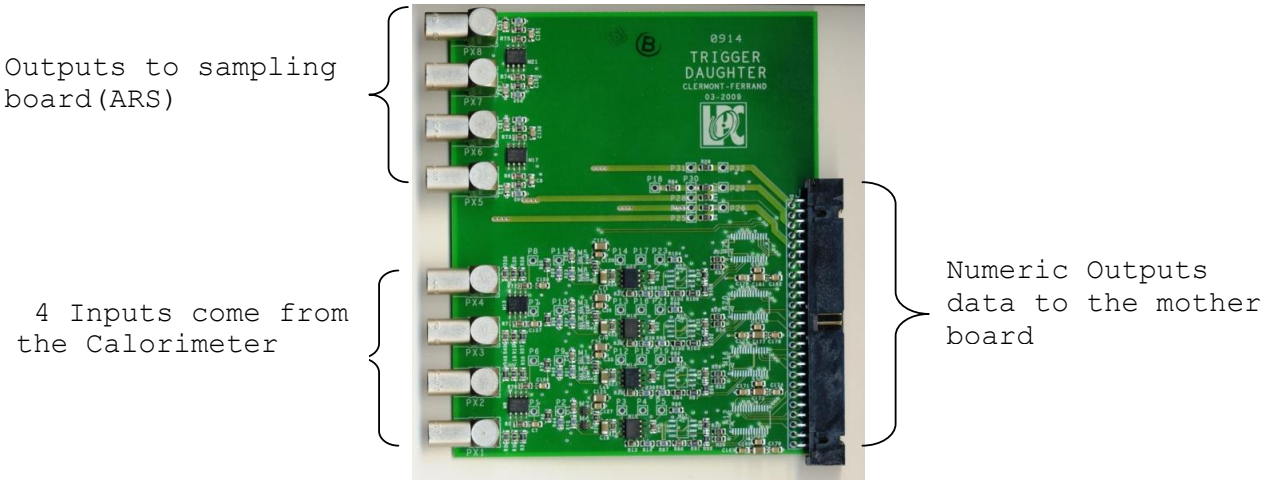


Figure 6 daughter electronic board

These boards permit to integrate positive and negative signal. The configuration signals are generated by the mother board (ctrl_FPGA).

2 type of signal are needed:
The gate for the integrator: this signal can have a parametric width and delay between the level 1 trigger. It's permit to adapt in time of the input signal arrival.
The multiplexing ADC output data are needed, because in goal to reduce the numbers of wire transit between the daughter board and the mother board, I have multiplexing the data (signal OE1/OE2/ OE3/OE4/CLK).

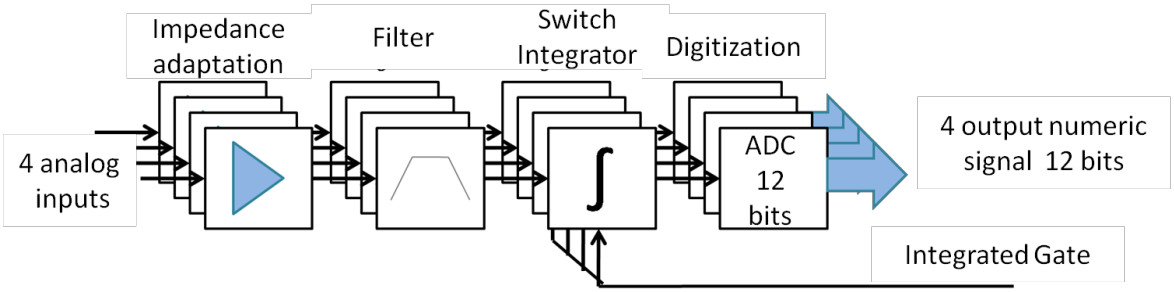


Figure 7 Daughter board diagram

The figure bellows shows in the result of integrated signal during a gate for a positive and a negative signal.

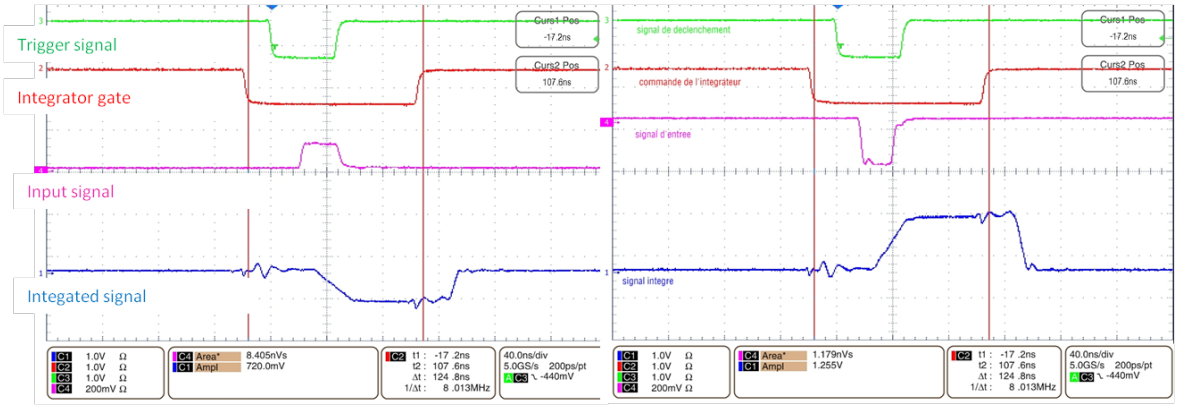


Figure 8 daughter board signal capture

The sampling is done all the time at each rising clock but the mother board acquires only the value at the end of the integrated gate.

The resolution of ADC versus integrator is around 12 pVs.

12pVs * 2048(positive part= half ADC) = 24 nVs

To have an idea :
1 ARS ADC step is 1ns * 0.6 mV ➔ 0.6 pVs

Amplitude max of a signal view by an ARS board is 600mV.
If the gate is 60 ns (width previously used for the 2010 experiment).

➔ max you have 60 ns * 600mV = 36 nVs,
But the gate never be full exept when you a very high signal.

A typical signal is around an integral 21000 ARS LSB

Equal to 12, 6nVS < 24 nVs offer by the trigger integration windows.

4. The mother boards (backplane)

5. The Trigger_Io_board

This board has for functionality to add more Numeric Inputs/outputs connectors on the front panel of the trigger box.

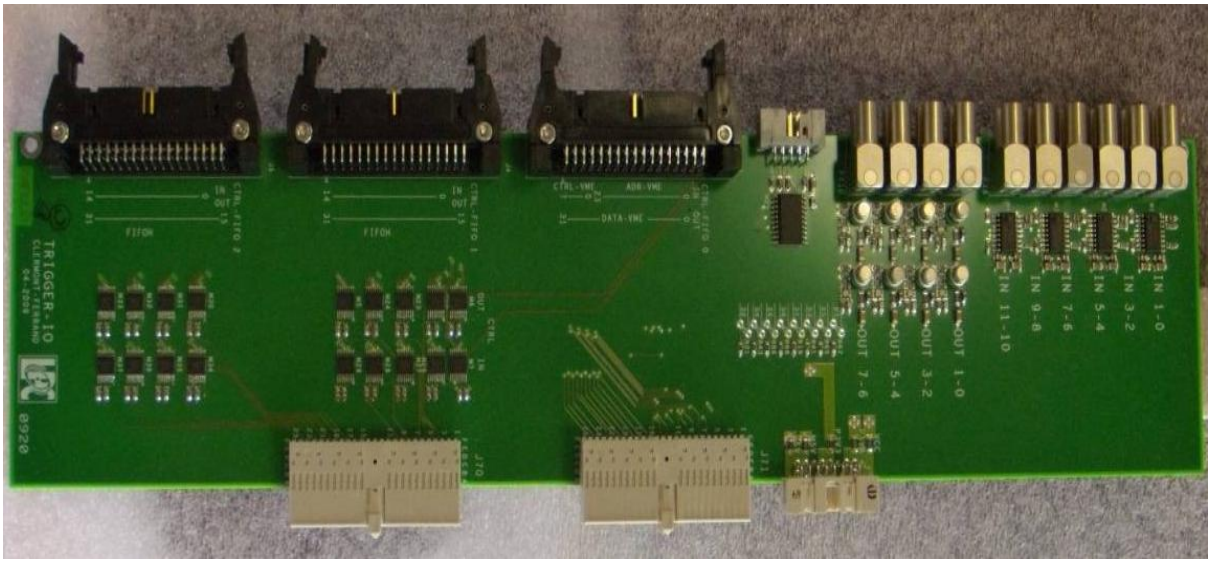


Figure 9 Tigger_IO Board

This board includes:
 12 NIM to TTL converter
 8 TTL to NIM converters
The Jtag input connector for the main jtag chain of the mother board.
The interface for the DATA signal between the mother board to the ribbon cable to the VME CTRL board.

And also the added JTAG chain connector for the logic unit FPGA of the mother board.

6. The Data27H board

This board has for functionality to add more Numeric Inputs on the front panel of the trigger box.
This added board is pug on the slot 27H of the mother board (previously used for daughter board spares)

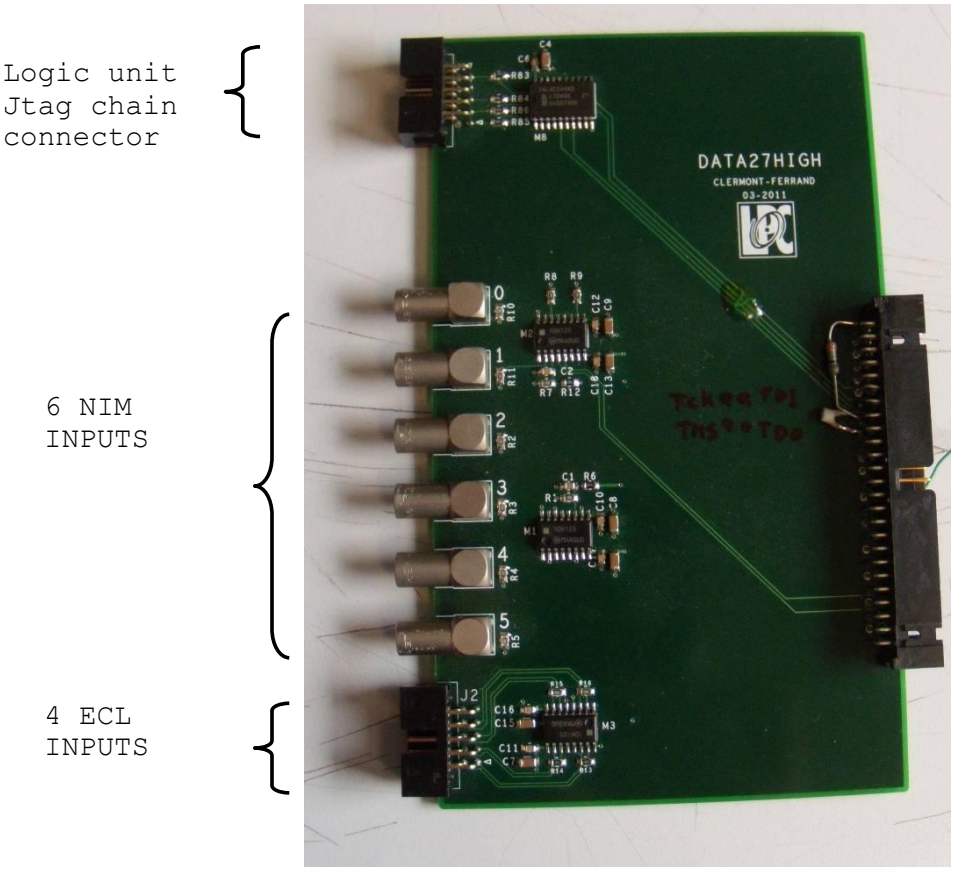


Figure 10 Data27H board

This board includes 6 NIM to TTL converter and 4 ECL to TTL converters. And also the added JTAG chain connector for the logic unit FPGA of the mother board.

7. The Data27L board

This board has for functionality to add more Numeric Outputs on the front panel of the trigger box.
This added board is pug on the slot 27L of the mother board (previously used for daughter board spares)

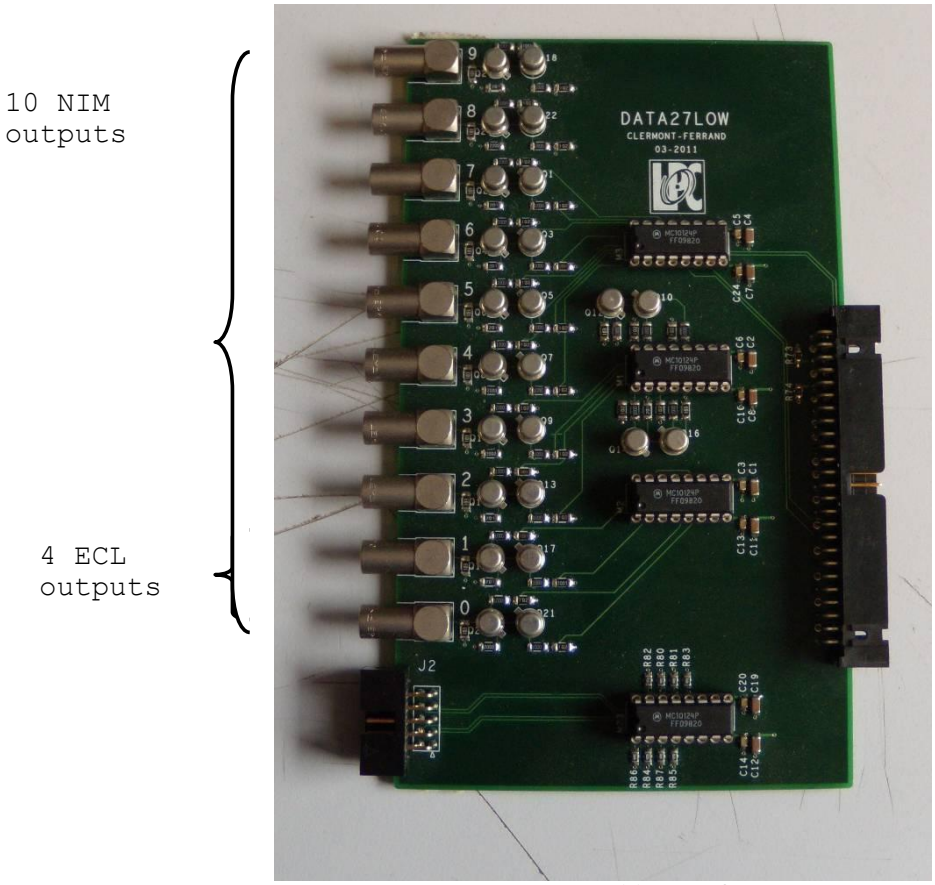
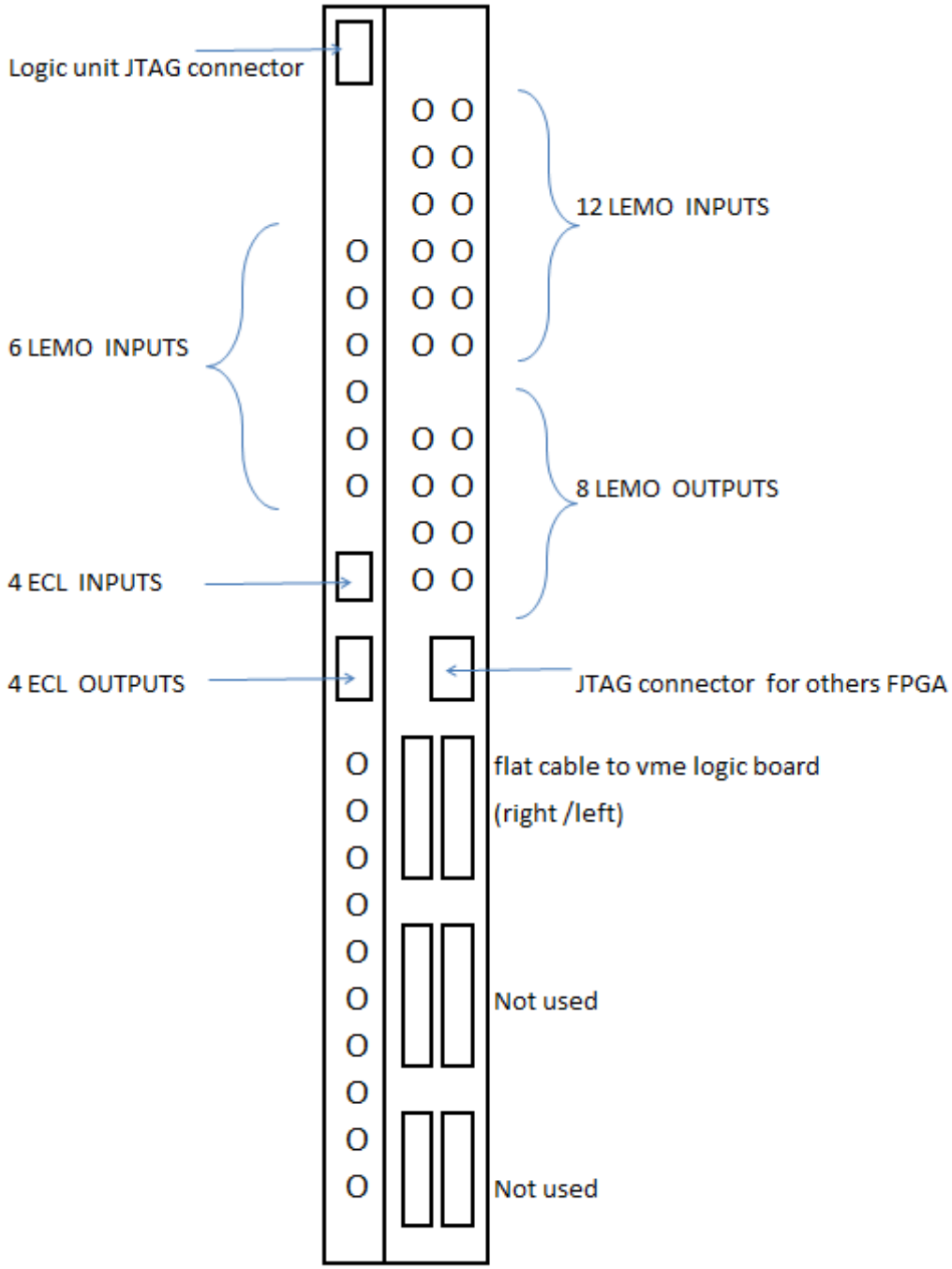


Figure 11 Data27L board

This board includes 10 TLL to NIM converter and 4 TTL to ECL converters.

8. Trigger Box connectors

Right part view include all the IO come from the boards: trigger_IO / Data27H and Data27L



The IO come from the Trigger_IO board are already defined.

It's the same of the previous trigger version
Part right:

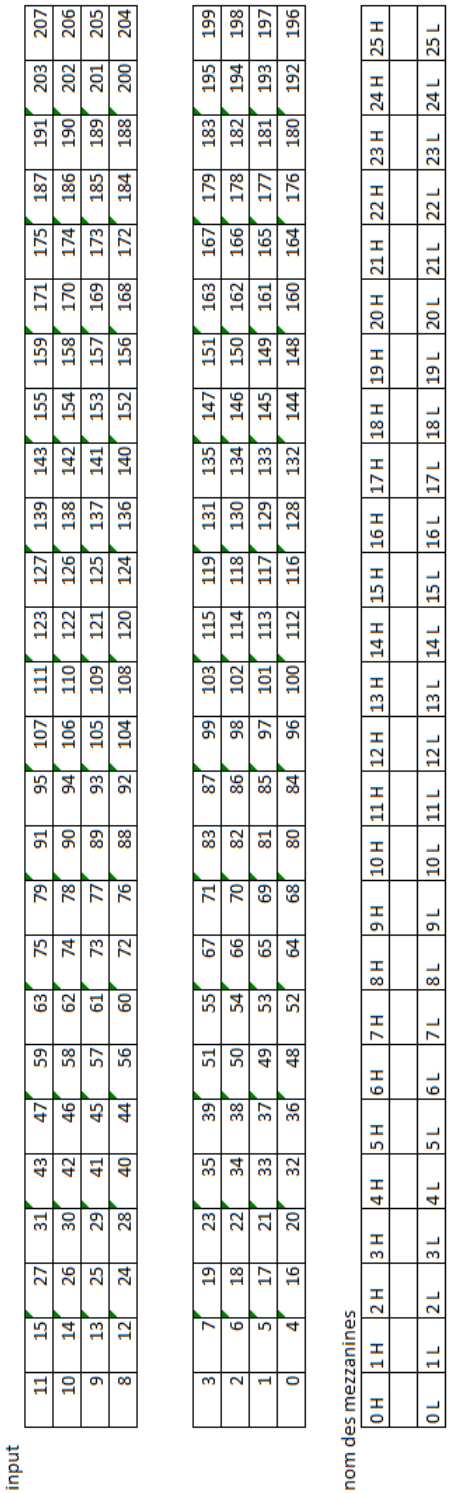
The adding input and outputs lemo and ecl are not defined at the

Calorimeter versus trigger inputs

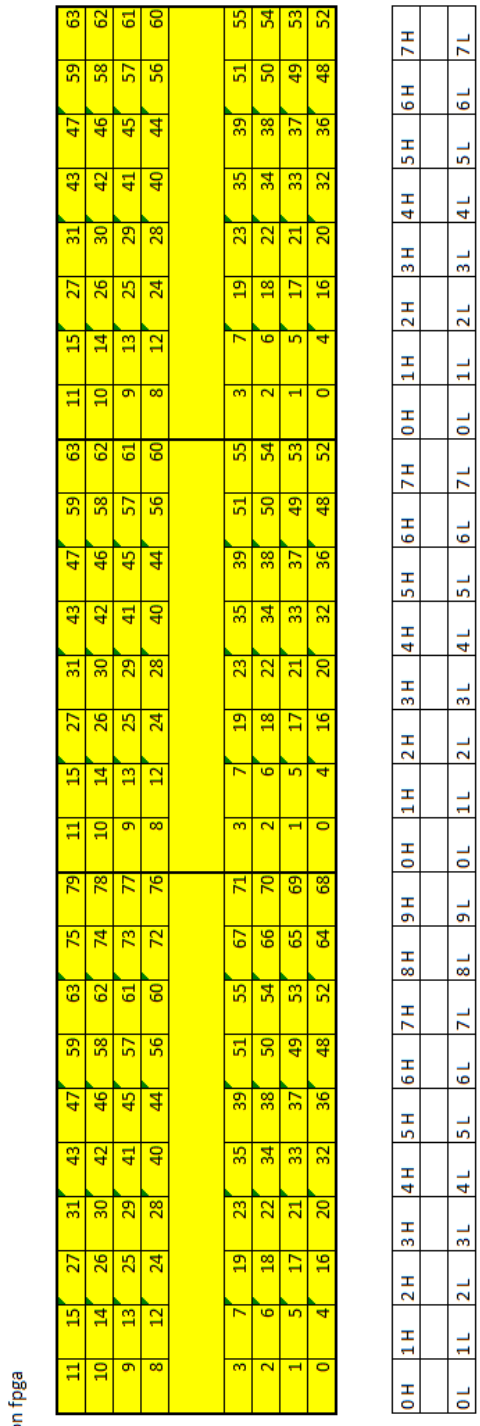
a. Calorimeter

15	31	47	63	79	95	111	127	143	159	175	191	207
14	30	46	62	78	94	110	126	142	158	174	190	206
13	29	45	61	77	93	109	125	141	157	173	189	205
12	28	44	60	76	92	108	124	140	156	172	188	204
11	27	43	59	75	91	107	123	139	155	171	187	203
10	26	42	58	74	90	106	122	138	154	170	186	202
9	25	41	57	73	89	105	121	137	153	169	185	201
8	24	40	56	72	88	104	120	136	152	168	184	200
7	23	39	55	71	87	103	119	135	151	167	183	199
6	22	38	54	70	86	102	118	134	150	166	182	198
5	21	37	53	69	85	101	117	133	149	165	181	197
4	20	36	52	68	84	100	116	132	148	164	180	196
3	19	35	51	67	83	99	115	131	147	163	179	195
2	18	34	50	66	82	98	114	130	146	162	178	194
1	17	33	49	65	81	97	113	129	145	161	177	193
0	16	32	48	64	80	96	112	128	144	160	176	192

b. Trigger inputs and board mezzanine reference



c. Trigger inputs and board mezzanine reference versus FPGA and VHDL assignments



d. Calorimeter versus FPGA

FPGA1 FPGA2 FPGA3

15	31	47	63	79	95	111	127	143	159	175	191	207
14	30	46	62	78	94	110	126	142	158	174	190	206
13	29	45	61	77	93	109	125	141	157	173	189	205
12	28	44	60	76	92	108	124	140	156	172	188	204
11	27	43	59	75	91	107	123	139	155	171	187	203
10	26	42	58	74	90	106	122	138	154	170	186	202
9	25	41	57	73	89	105	121	137	153	169	185	201
8	24	40	56	72	88	104	120	136	152	168	184	200
7	23	39	55	71	87	103	119	135	151	167	183	199
6	22	38	54	70	86	102	118	134	150	166	182	198
5	21	37	53	69	85	101	117	133	149	165	181	197
4	20	36	52	68	84	100	116	132	148	164	180	196
3	19	35	51	67	83	99	115	131	147	163	179	195
2	18	34	50	66	82	98	114	130	146	162	178	194
1	17	33	49	65	81	97	113	129	145	161	177	193
0	16	32	48	64	80	96	112	128	144	160	176	192

e. Calorimeter versus FPGA and VHDL assignments

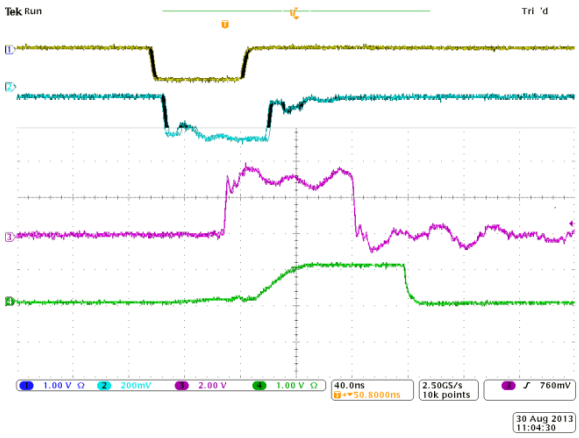
FPGA1 FPGA2 FPGA3

15	31	47	63	79	15	31	47	63	15	31	47	63
14	30	46	62	78	14	30	46	62	14	30	46	62
13	29	45	61	77	13	29	45	61	13	29	45	61
12	28	44	60	76	12	28	44	60	12	28	44	60
11	27	43	59	75	11	27	43	59	11	27	43	59
10	26	42	58	74	10	26	42	58	10	26	42	58
9	25	41	57	73	9	25	41	57	9	25	41	57
8	24	40	56	72	8	24	40	56	8	24	40	56
7	23	39	55	71	7	23	39	55	7	23	39	55
6	22	38	54	70	6	22	38	54	6	22	38	54
5	21	37	53	69	5	21	37	53	5	21	37	53
4	20	36	52	68	4	20	36	52	4	20	36	52
3	19	35	51	67	3	19	35	51	3	19	35	51
2	18	34	50	66	2	18	34	50	2	18	34	50
1	17	33	49	65	1	17	33	49	1	17	33	49
0	16	32	48	64	0	16	32	48	0	16	32	48

moment.

9. ANNEXES

a. Typical trigger signals



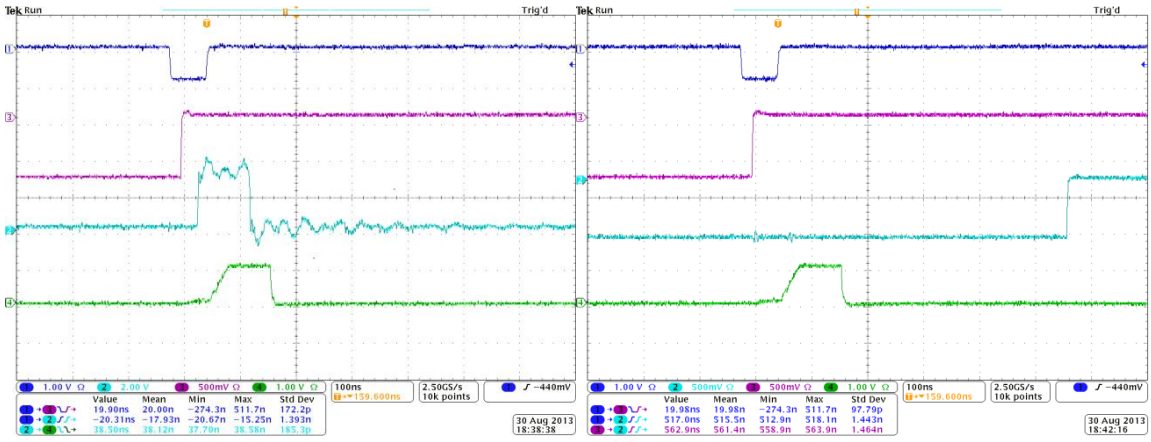
1 - trigger cosmic

2 - Analog input signal (example channel 16)

3 - gate for integrated signal

4 - analog integrated signal

Timing ARS_stop/ ARS_start /Gate /signal integer



1 –cosmic trigger
2 – Ars_stop
3 – Gate (left plot) – ARS_start (right)
4 – analog integrated signal